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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,650	12/31/2001	Shiv Kaushik	042390.P13636	9232

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/039,650	KAUSHIK ET AL.
	Examiner	Art Unit
	Charles A Harkness	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/05/02, 03/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS rcvd on 08/12/03, 06/17/04*.

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Oath/Declaration as received on 04/16/02; Information Disclosure Statement as received on 08/05/02; Information Disclosure Statement as received on 03/21/03; Information Disclosure Statement as received on 08/12/03; and Information Disclosure Statement as received on 06/17/04.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-30 rejected under 35 U.S.C. 102(e) as being anticipated by Emer et al., U.S. Patent Number 6,493,741 (herein referred to as Emer).

5. Referring to claims 1, 12 and 18 Emer has taught an article comprising a machine readable medium storing instructions that, if executed by a machine, cause the machine to perform a plurality of operations comprising:

specifying a monitor address;

suspending a thread until a monitor break event occurs;

testing whether the monitor break event is a write to the monitor address;

if the monitor break event is not the write to the monitor address, then suspending the thread again (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50).

6. Referring to claims 2 and 13 Emer has taught wherein suspending the thread again comprises returning to specifying the monitor address (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50).

7. Referring to claims 3 and 14 Emer has taught wherein specifying the monitor address comprises executing a MONITOR instruction and wherein suspending the thread until the monitor break event occurs comprises executing an MWAIT instruction (Emer column 5 lines 28-40).

8. Referring to claims 4 and 15 Emer has taught wherein said plurality of operations further comprise, after specifying the monitor address and before suspending the thread: testing whether data at the monitor address has changed (Emer figure 9 column 1 1 line 1-column 12 line 35).

9. Referring to claims 5 and 16 Emer has taught wherein specifying the monitor address comprises executing an instruction with an operand chosen from a set consisting of a linear address, a virtual address, a physical address, and a relative address (Emer column 5 lines 28-40).

10. Referring to claims 6 and 17 Emer has taught wherein the operand is one of a second set consisting of an explicit operand and an implicit operand (Emer column 5 lines 28-40).

11. Referring to claim 7 Emer has taught wherein said monitor address specifies a cache line (Emer figure 3 column 6 lines 12-30, column 7 lines 51-65).

12. Referring to claims 8 and 19 Emer has taught wherein said plurality of operations further comprise providing a second operand as a mask operand to control which events are monitor break events (Emer column 11 line 38-column 12 line 6, table in column 9).

13. Referring to claim 9 Emer has taught an article comprising a machine readable medium storing instructions that, if executed by a machine, cause the machine to perform operations comprising:

programming a monitor with a monitor address corresponding to a cache line of at least one work location (Emer column 5 lines 28-40; figure 3 column 6 lines 12-30, column 7 lines 51-65);

suspending a thread until a monitor break event occurs (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50);

testing whether the at least one work location indicates a first task is ready to execute (Emer figure 3 figure 8, column 3 lines 28-67, column 14 lines 27-50, column 5 line 51-column 6 line 67);

testing whether the at least one work location indicates a second task is ready to execute (Emer figure 3 figure 8, column 3 lines 28-67, column 14 lines 27-50, column 5 line 51-column 6 line 67);

if neither the first task nor the second task is ready to execute, then returning to suspending the thread (Emer figure 3 figure 8, column 3 lines 28-67, column 14 lines 27-50, column 5 line 51-column 6 line 67).

14. Referring to claim 10 Emer has taught wherein returning to suspending the thread until the monitor break event occurs further comprises re-programming the monitor with the monitor address prior to suspending the thread (Emer figure 9 column 11 line 1-column 12 line 35, column 5 lines 28-40).

15. Referring to claim 11 Emer has taught wherein returning to suspending the thread comprises returning to programming the monitor with the monitor address (Emer figure 9 column 11 line 1-column 12 line 35, column 5 lines 28-40).

16. Referring to claim 20 Emer has taught a system comprising: a processor;

a monitor to generate a monitor break event in response to a memory access to a monitor address (Emer figure 2 figure 8, column 3 lines 28-67, column 14 lines 27-50);

event detect logic to detect an of a plurality of monitor break events; a memory to store a loop in a first thread executable by said processor to specify said monitor address and to repeatedly suspend said first thread after monitor break events until the memory access to the monitor address occurs (Emer figure 2 figure 8, column 3 lines 28-67, column 14 lines 27-50).

17. Referring to claim 21 Emer has taught wherein said loop comprises:

a first instruction to specify the monitor address; a second instruction to suspend said first thread (Emer column 5 lines 28-40).

18. Referring to claim 22 Emer has taught wherein said loop further comprises a test after said first instruction to determine whether data at the monitor address has changed after

execution of the first instruction but before execution of the second instruction, wherein said loop exits without execution of the second instruction if data at the monitor address has changed (Emer figure 9 column 11 line 1-column 12 line 35).

19. Referring to claim 23 Emer has taught wherein said loop further comprises a test after said first instruction to determine whether data at the monitor address has changed after execution of the second instruction wherein said loop performs another iteration if data at the monitor address has not changed (Emer figure 2 figure 8, column 3 lines 28-67, column 14 lines 27-50).

20. Referring to claim 24 Emer has taught wherein said loop comprises: a test to determine whether a work location in a first cache line indicated by the monitor address contains a first value, wherein a first routine is executed if said work location contains the first value (Emer figure 3 figure 8, column 3 lines 28-67, column 14 lines 27-50, column 5 line 51-column 6 line 67);

a second test to determine whether the work location in said first cache line contains a second value, wherein a second routine is executed if said work location contains the second value (Emer figure 3 figure 8, column 3 lines 28-67, column 14 lines 27-50, column 5 line 51-column 6 line 67);

an instruction to suspend said first thread if said work location does not contain said first value and said work location does not contain said second value (Emer figure 3 figure 8, column 3 lines 28-67, column 14 lines 27-50, column 5 line 51-column 6 line 67).

21. Referring to claim 25 Emer has taught a system comprising: a processor;

a monitor (Emer figure 2 number 109);

a memory to store an idle loop in a first thread executable by said processor to perform operations comprising (Emer figures 2-3 and 6):

specifying a monitor address; suspending said first thread until a monitor break event occurs;

testing whether the monitor break event is a write to the monitor address;

if the monitor break event is not the write to the monitor address, then returning to specifying the monitor address (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50).

22. Referring to claim 26 Emer has taught wherein specifying the monitor address comprises executing a first instruction and wherein suspending the thread until the monitor break event occurs comprises executing a second instruction (Emer column 5 lines 28-40).

23. Referring to claim 27 Emer has taught wherein said operations further comprise, after specifying the monitor address and before suspending the thread: testing whether data at the monitor address has changed (Emer figure 9 column 11 line 1-column 12 line 35).

24. Referring to claim 28 Emer has taught a method comprising: executing a first instruction in a first thread that specifies a monitor address (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50; column 5 lines 28-40);

executing a second instruction in said first thread to suspend said first thread until a write access implicating said monitor address or an interrupt occurs (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50; column 5 lines 28-40);

executing a plurality of instructions in a second thread (Emer figure 1 column 1 line 66-column 2 line 34);

after the write access or the interrupt occurs, testing whether a data element associated with said monitor address has changed (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50; column 5 lines 28-40);

returning to executing the second instruction if the data element has not changed.

25. Referring to claim 29 Emer has taught wherein returning to executing the second instruction comprises returning to executing the first instruction and continuing on to executing the second instruction (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50; column 5 lines 28-40).

26. Referring to claim 30 Emer has taught further comprising testing whether the data element associated with said monitor address has changed prior to executing said second instruction (Emer figure 9 column 11 line 1-column 12 line 35).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Zhang et al., U.S. Patent Number 6,457,082, has taught break event generation while switching between modes of operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579 and 571-272-4167 after 10/12/04. The examiner can normally be reached on 8Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Examiner

Art Unit 2183

September 29, 2004

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